What is claimed is:

1. A semiconductor device comprising: regions for forming a plurality of functional blocks; and a region for forming wiring layers for connecting the functional blocks, wherein each of the regions for forming the functional blocks includes a multilayer wiring, and the region for forming the wiring layers for connecting adjacent functional blocks includes a coaxial line comprised of a signal line and a ground line surrounding the signal line via an insulating film.

2. A semiconductor device according to claim 1, wherein a bottom surface of any wiring in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the coaxial line provided in the region for forming the wiring layers for connecting the functional blocks.

3. A semiconductor device comprising: regions for forming a plurality of functional blocks; and a region for forming wiring layers for connecting the functional blocks, wherein each of the regions for forming the functional blocks includes a multilayer wiring, and the region for forming the wiring layers for connecting the functional blocks includes a transmission line comprising a signal line and ground lines or

power source lines formed above and below the signal line, respectively to sandwich the signal line via an insulating film.

4. A semiconductor device according to claim 3, wherein a bottom surface of any wiring in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the ground line or power source line provided in the region for forming the wiring layers for connecting the functional blocks.

5. A semiconductor device comprising: regions for forming a plurality of functional blocks; and a region for forming wiring layers for connecting the functional blocks, wherein each of the regions for forming the functional blocks includes a multilayer wiring, and the region for forming the wiring layers for connecting the functional blocks includes wiring layers thicker than those in the functional blocks, and a bottom surface of any wiring in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the wiring layer provided in the region for forming the wiring layers for connecting the functional blocks.

6. A method of manufacturing a semiconductor device having regions for forming a plurality of functional blocks and

a region for forming wiring layers for connecting the functional blocks, the method comprising the steps of:

forming a groove corresponding to a first wiring layer in an underlying insulating film in the region for forming the functional block and at the same time, forming a groove corresponding to a lower part of a ground line which surrounds a single line to form a coaxial line in an underlying insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a first wiring layer and a lower part of the ground line;

depositing a first insulating film capable of preventing diffusion of the wiring material, depositing a first interlayer insulating film, and then forming a hole for connecting the first wiring layer with a second wiring layer in the first interlayer insulating film in the region for forming the functional block and at the same time, forming grooves corresponding to side parts of the ground line in the first interlayer insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a groove corresponding to a second wiring

layer in the region for forming the functional block, and at the same time, forming a groove corresponding to a signal line in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a second wiring layer, side parts of the ground line and a signal line;

depositing a second insulating film capable of preventing diffusion of the wiring material, depositing a second interlayer insulating film, and then forming a hole for connecting the second wiring layer with a third wiring layer in the second interlayer insulating film in the region for forming the functional block and at the same time, forming grooves corresponding to side parts of the ground line in the second interlayer insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a groove corresponding to a third wiring layer in the second interlayer insulating film in the region for forming the functional block and at the same time, forming a groove corresponding to an upper part of the ground line in the second interlayer insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a third wiring layer and an upper part of the ground line; and

depositing a third insulating film capable of preventing diffusion of the wiring material.

7. A method of manufacturing a semiconductor device having regions for forming a plurality of functional blocks and a region for forming wiring layers for connecting the functional blocks, the method comprising the steps of:

forming a groove corresponding to a first wiring layer in an underlying interlayer insulating film in the region for forming the functional block and at the same time, forming a groove corresponding to a lower ground line or power source line in an underlying interlayer insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a first wiring layer and the lower ground line or power source line;

depositing a first insulating film capable of preventing diffusion of the wiring material, depositing a first interlayer insulating film, and then forming a hole for connecting the first wiring layer with a second wiring layer in the first interlayer insulating film in the region for forming the functional block;

forming a groove corresponding to a second wiring layer in the region for forming the functional block and at the same time, forming a groove corresponding to a signal line in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a second wiring layer and a signal line;

depositing a second insulating film capable of preventing diffusion of the wiring material, depositing a second interlayer insulating film, and then forming a hole for connecting the second wiring layer with a third wiring layer in the second interlayer insulating film in the region for forming the functional block;

forming a groove corresponding to a third wiring layer in the region for forming the functional block and at the same time, forming a groove corresponding to an upper ground line

or power source line in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a third wiring layer and an upper ground line or power source line; and

depositing a third insulating film capable of preventing diffusion of the wiring material.

8. A method of manufacturing a semiconductor device having regions for forming a plurality of functional blocks and a region for forming wiring layers for connecting the functional blocks, the method comprising the steps of:

forming a groove corresponding to a first wiring layer in an underlying insulating film in the region for forming the functional block and at the same time, forming a groove corresponding to a lower part of a ground line which surrounds a single line to form a coaxial line in an underlying insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical

polishing so that the wiring material layer is left only in the grooves, thereby forming a first wiring layer and a lower part of the ground line;

depositing a first insulating film capable of preventing diffusion of the wiring material, depositing a first interlayer insulating film, and then forming a hole for connecting the first wiring layer with a second wiring layer in the first interlayer insulating film in the region for forming the functional block and at the same time, forming grooves corresponding to side parts of the ground line in the first interlayer insulating film in the region for forming wiring layers for connecting the functional blocks;

forming a groove corresponding to a second wiring layer in the first interlayer insulating film in the region for forming the functional block and at the same time, forming a groove corresponding to a signal line in the first interlayer insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a second wiring layer, side parts of the ground line and a signal line;

depositing a second insulating film capable of

preventing diffusion of the wiring material, depositing a second interlayer insulating film, and then forming a hole for connecting the second wiring layer with a third wiring layer in the second interlayer insulating film in the region for forming the functional block and at the same time, forming grooves corresponding to side parts of the ground line and a signal line in the second interlayer insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a groove corresponding to a third wiring layer in the second interlayer insulating film in the region for forming the functional block and at the same time, forming grooves corresponding to side parts of the ground line and a signal line in the second interlayer insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a third wiring layer and a signal line;

depositing a third insulating film capable of preventing diffusion of the wiring material, depositing a third interlayer insulating film, and then forming a hole for connecting the third wiring layer with a fourth wiring layer in the third interlayer insulating film in the region for forming the

functional block and at the same time, forming grooves corresponding to side parts of the ground line in the third insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a groove corresponding to a fourth wiring layer in the third interlayer insulating film in the region for forming the functional block and at the same time, forming a groove corresponding to an upper part of the ground line in the third interlayer insulating film in the region for forming the wiring layers for connecting the functional blocks;

forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a fourth wiring layer and an upper part of the ground line; and

depositing a fourth insulating film capable of preventing diffusion of the wiring material.

9. A method of manufacturing a semiconductor device having regions for forming a plurality of functional blocks and a region for forming wiring layers for connecting the functional blocks, the method comprising the steps of:

forming a groove corresponding to a first wiring layer in an underlying insulating film in the region for forming the

functional block;

forming a barrier metal layer in the groove by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a first wiring layer;

depositing a first insulating film capable of preventing diffusion of the wiring material, depositing a first interlayer insulating film, and then forming a hole for connecting the first wiring layer with a second wiring layer in the first interlayer insulating film in the region for forming the functional block and at the same time, forming a groove corresponding to a signal line in the first interlayer insulating film in the region for forming wiring layers for connecting the functional blocks;

forming a groove corresponding to a second wiring layer in the first interlayer insulating film in the region for forming the functional block, forming a barrier metal layer in the grooves by Damascene process, forming a wiring material layer, and then subjecting the wiring material layer to chemical mechanical polishing so that the wiring material layer is left only in the grooves, thereby forming a second wiring layer and a signal line; and

depositing a second insulating film capable of preventing diffusion of the wiring material.